

CLAIMS

What is claimed is:

1. Circuitry, comprising:

5 at least one first timing circuit including a first input, a first output, and a current source, the first input being electrically coupled to the first output, the first input being coupleable to at least one capacitor and at least one clamping element,

10 wherein the current source is operative to apply a constant current to the capacitor, thereby generating a ramped timing signal at the first input and providing the ramped timing signal to the first output electrically coupled to the first input, and

15 wherein the timing signal provided at the first output of the first timing circuit has an associated first state in the event only the capacitor is coupled between the first input and ground, and an associated second state in the event the clamping element is coupled
20 between the first input and ground; and

 a second circuit operable in a plurality of modes having at least one control input and a second output, the control input being electrically coupled to the first output of the first timing circuit,

25 wherein the second circuit is configured to operate in a first mode in the event the timing signal having the associated first state is provided to the control input via the first output, and to operate in a second mode in the event the timing signal having the associated second

state is provided to the control input via the first output.

2. The circuitry of claim 1 wherein the first timing
5 circuit comprises a soft-start circuit.

3. The circuitry of claim 2 wherein the soft-start
circuit is configured to generate a soft-start signal
having an associated soft-start time (T_{ss}), and wherein T_{ss}
10 is determined by a predetermined value of the capacitor.

4. The circuitry of claim 3 wherein T_{ss} is determined by
a formula

$$C_{ssx}(\text{Farads}) = T_{ss}(\text{sec}) \times 2.3 \times 10^{-6}.$$

15

5. The circuitry of claim 1 wherein the second circuit
comprises an oscillator.

6. The circuitry of claim 5 wherein the oscillator is
20 configured to generate a plurality of first switching
frequencies in the event the timing signal having the
associated first state is provided to the control input,
and to generate a plurality of second switching
frequencies in the event the timing signal having the
25 associated second state is provided to the control input.

7. The circuitry of claim 6 wherein the plurality of
first switching frequencies includes at least one first
low switching frequency and at least one first high

switching frequency, wherein the oscillator is configured to generate the first low switching frequency during a first time period, and wherein the oscillator is configured to generate the first high switching frequency during a second time period subsequent to the first time period.

8. The circuitry of claim 6 wherein the plurality of second switching frequencies includes at least one second low switching frequency and at least one second high switching frequency, wherein the oscillator is configured to generate the second low switching frequency during a first time period, and wherein the oscillator is configured to generate the second high switching frequency during a second time period subsequent to the first time period.

9. A method of generating at least one soft-start signal and at least one switching frequency, comprising the steps of:

providing at least one soft-start circuit including a first input, a first output, and a current source, the first input being electrically coupled to the first output, the first input being coupleable to at least one capacitor and at least one resistor;

applying a constant current to the capacitor by the current source, thereby generating a ramped soft-start signal at the first input and providing the ramped soft-start signal to the first output electrically coupled to

the first input, wherein the soft-start signal provided at the first output of the soft-start circuit has an associated first state in the event only the capacitor is coupled between the first input and ground, and an
5 associated second state in the event the resistor is coupled between the first input and ground;

providing an oscillator having at least one control input and a second output, the control input being electrically coupled to the first output of the soft-
10 start circuit;

in the event the soft-start signal having the associated first state is provided to the control input via the first output, generating at least one first switching frequency by the oscillator; and

15 in the event the soft-start signal having the associated second state is provided to the control input via the first output, generating at least one second switching frequency by the oscillator.

20 10. The method of claim 9 wherein the applying step includes generating a soft-start signal having an associated soft-start time (T_{ss}) by the soft-start circuit, and determining T_{ss} by a predetermined value of the capacitor.

25 11. The method of claim 10 wherein the applying step includes determining T_{ss} by a formula

$$C_{ssx}(\text{Farads}) = T_{ss}(\text{sec}) \times 2.3 \times 10^{-6}.$$

12. The method of claim 9 wherein the first generating step includes generating a plurality of first switching frequencies in the event the soft-start signal having the associated first state is provided to the control input, and wherein the second generating step includes generating a plurality of second switching frequencies in the event the soft-start signal having the associated second state is provided to the control input.
13. The method of claim 12 wherein the plurality of first switching frequencies includes at least one first low switching frequency and at least one first high switching frequency, and wherein the first generating step includes generating the first low switching frequency during a first time period and generating the first high switching frequency during a second time period subsequent to the first time period.
14. The method of claim 12 wherein the plurality of second switching frequencies includes at least one second low switching frequency and at least one second high switching frequency, and wherein the second generating step includes generating the second low switching frequency during a first time period and generating the second high switching frequency during a second time period subsequent to the first time period.

15. A switch mode power converter configured to receive an input voltage and to generate an output voltage, comprising:

at least one soft-start circuit including a first
5 input, a first output, and a current source, the first
input being electrically coupled to the first output, the
first input being coupleable to at least one capacitor
and at least one resistor, wherein the current source is
operative to apply a constant current to the capacitor,
10 thereby generating a ramped soft-start signal at the
first input and providing the ramped soft-start signal to
the first output electrically coupled to the first input,

wherein the soft-start signal provided at the first
output of the soft-start circuit has an associated first
15 state in the event only the capacitor is coupled between
the first input and ground, and an associated second
state in the event the resistor is coupled between the
first input and ground; and

an oscillator having at least one control input and
20 a second output, the control input being electrically
coupled to the first output of the soft-start circuit,

wherein the oscillator is configured to generate a
plurality of first switching frequencies in the event the
soft-start signal having the associated first state is
25 provided to the control input via the first output, and
to generate a plurality of second switching frequencies
in the event the soft-start signal having the associated
second state is provided to the control input via the
first output.

16. The converter of claim 15 wherein the plurality of first switching frequencies includes at least one first low switching frequency and at least one first high switching frequency, and wherein the oscillator is configured to generate the first low switching frequency during a first time period, and to generate the first high switching frequency during a second time period subsequent to the first time period in the event the output voltage has stabilized.

17. The converter of claim 15 wherein the plurality of second switching frequencies includes at least one second low switching frequency and at least one second high switching frequency, and wherein the oscillator is configured to generate the second low switching frequency during a first time period, and to generate the second high switching frequency during a second time period subsequent to the first time period in the event the output voltage has stabilized.

18. A method of operating a switch mode power converter, the converter including at least one soft-start circuit and an oscillator, the soft-start circuit including a first input, a first output, and a current source, the first input being electrically coupled to the first output, the oscillator having at least one control input and a second output, the control input being electrically

coupled to the first output of the soft-start circuit,
comprising the steps of:

receiving an input voltage and generating an output
voltage by the switch mode power converter;

5 applying a constant current to the capacitor by the
current source, thereby generating a ramped soft-start
signal at the first input and providing the ramped soft-
start signal to the first output electrically coupled to
the first input, wherein the soft-start signal provided
10 at the first output of the soft-start circuit has an
associated first state in the event only a capacitor is
coupled between the first input and ground, and an
associated second state in the event a resistor is
coupled between the first input and ground;

15 in the event the soft-start signal having the
associated first state is provided to the control input
via the first output, generating a plurality of first
switching frequencies by the oscillator; and

20 in the event the soft-start signal having the
associated second state is provided to the control input
via the first output, generating a plurality of second
switching frequencies by the oscillator.

19. The method of claim 18 wherein the plurality of
25 first switching frequencies includes at least one first
low switching frequency and at least one first high
switching frequency, and wherein the first generating
step includes generating the first low switching
frequency during a first time period and generating the

first high switching frequency during a second time period subsequent to the first time period in the event the output voltage has stabilized.

- 5 20. The method of claim 18 wherein the plurality of
second switching frequencies includes at least one second
low switching frequency and at least one second high
switching frequency, and wherein the second generating
step includes generating the second low switching
10 frequency during a first time period and generating the
second high switching frequency during a second time
period subsequent to the first time period in the event
the output voltage has stabilized.